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TFT LCD Approval Specification

MODEL NO.: N154C1 -L01

Customer : ASUS

Approved by : _____

Note :

記錄	工作	審核	角色	投票
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2006-08-04 18:47:08 CST	Approve by Director	teren_lin(林添仁/56910/36064)	Director	Accept

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	Aug. 30. '05	All	All	Tentative specification first issued.
Ver 1.0	Oct. 13. '05	All	All	Preliminary specification first issued.
		4.	1.4.	Modify Surface Treatment
		10.	3.2	Modify BACKLIGHT UNIT spec.
		17~19	5.5	Modify EDID DATA STRUCTURE
		22.	7.2.	Modify OPTICAL SPECIFICATIONS
		27.	9.	Packing specification changed.
Ver 1.1	Dec. 05. '05	All	All	Preliminary specification updated.
		6.	2.1	Modify ABSOLUTE RATINGS OF ENVIRONMENT.
		7.	2.2	Modify 2.2.2 BACKLIGHT UNIT
		10.	3.2	Modify 3.2 BACKLIGHT UNIT
		22.	7.2	Modify 7.2 OPTICAL SPECIFICATIONS
		28.	10.2	Modify 10.2 CARTON LABEL
Ver 3.0	Jun. 15. '06	30	-	Module drawing update
Ver 3.1	Jul. 20. '06	7	3.1	Electrical characteristics/TFT LCD module
		12	5.1	Input terminal pin assignment/TFT LCD module
		17	6.1	Interface timing/input signal timing specifications
Ver 3.2	Aug. 04. '06	28		Outline drawing update

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1 GENERAL DESCRIPTION

1.1 OVERVIEW

N154C1 -L01 is a 15.4" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1440 x 900 WXGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and light weight
- WXGA+ (1440 x 900 pixels) resolution
- DE (Data Enable) only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- Support EDID Structure Version 1.3

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

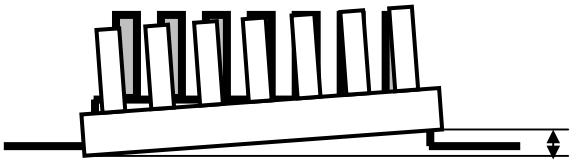
Item	Specification	Unit	Note
Outline Dimension	344(W) x 222 (H)	mm	(1)
Active Area	331.56 (H) x 207.225 (V)	mm	
Bezel Opening Area	335 (H) x 210.7 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.23025 (H) x 0.23025 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hardness (3H), Glare ,Reflection=1.2 %	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	343.5	344	344.5	mm	(1)
	Vertical(V)	221.5	222	222.5	mm	
	Depth(D)	---	---	6.2	mm	
Weight		---	530	540	g	-
I/F connector mounting position		The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



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2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

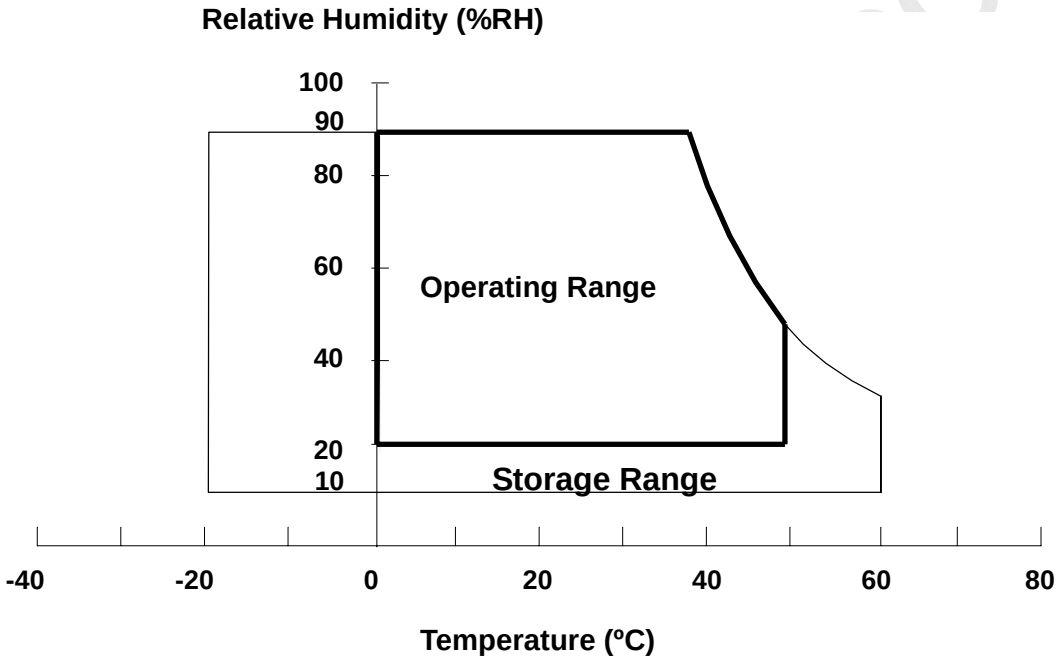
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 50 ºC max.

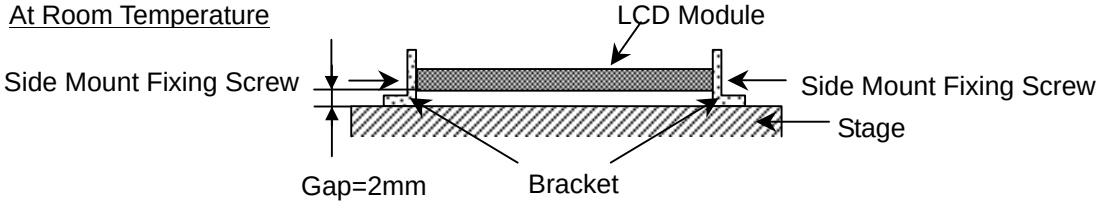


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~200 Hz, 0.5hr/cycle 1cycle for X,Y,Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	Vcc+0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	-	2.5K	V_{RMS}	(1), (2), I_L = 6.0 mA
Lamp Current	I_L	2.0	7.0	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	50	60	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

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CHI MEI OPTOELECTRONICS CORP.

Doc. No.: 14067606
Issued Date: Aug.04, 2006
Model No.: N154C1 -L01

Approval

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

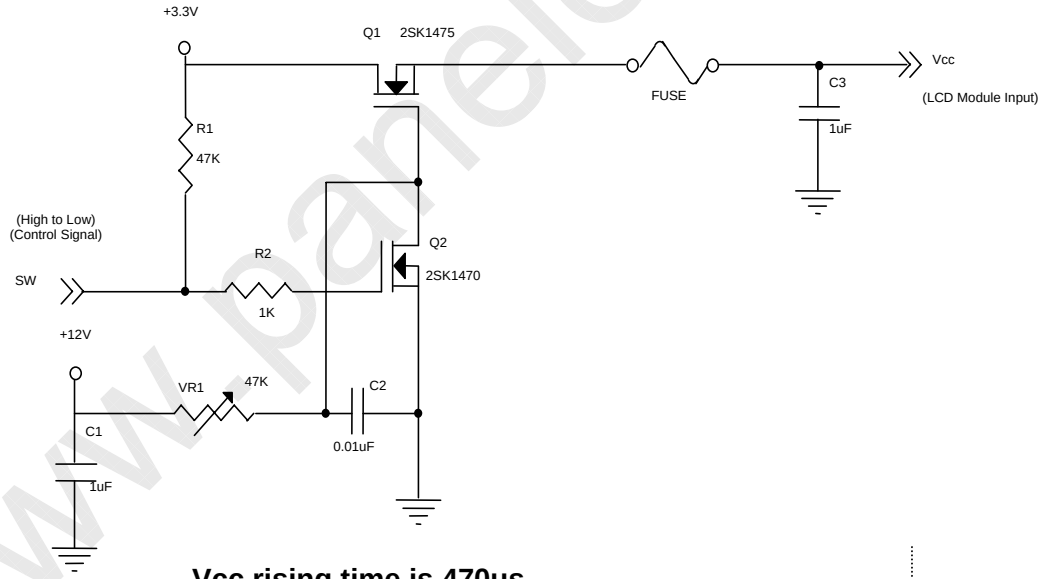
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}		50		mV	-
Rush Current		I_{RUSH}			1.5	A	(2)
Initial Stage Current		I_{IS}			1.0	A	(2)
Power Supply Current	White	Icc		270	320	mA	(3)a
	Black			410	470	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$			+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100			mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125		1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100		600	mV	(5)
Terminating Resistor		R_T		100		Ohm	
Power per EBL WG		P_{EBL}	-	3.1	-	W	(4)

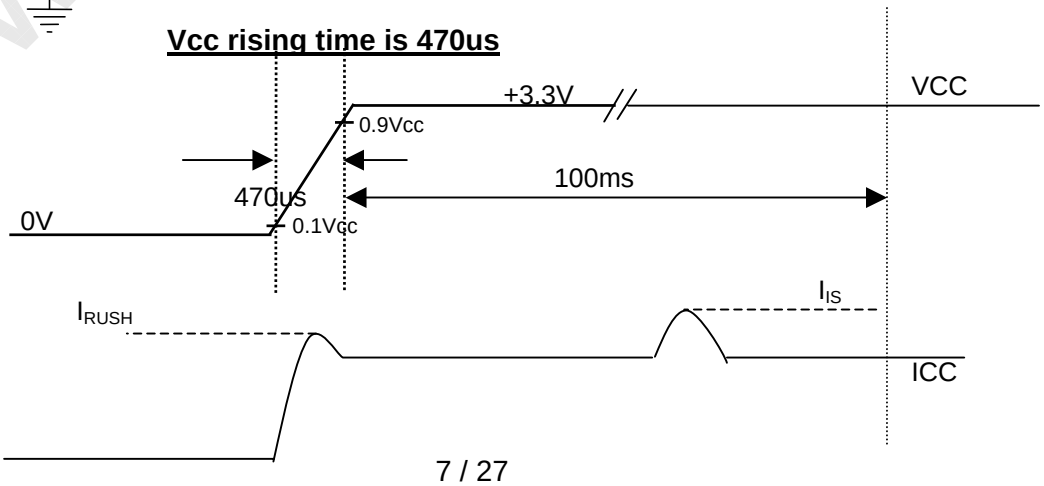
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.





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Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

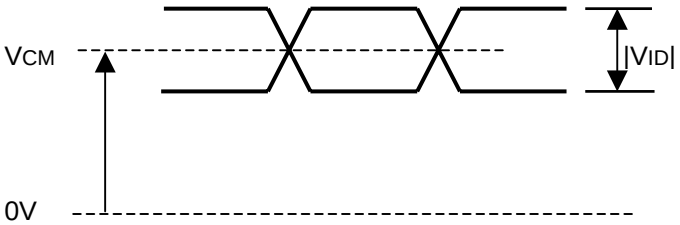
(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

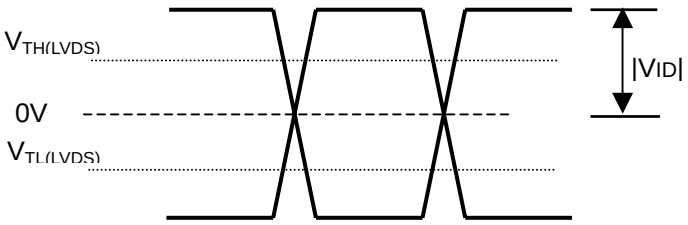
(d) The inverter used is provided from _Logah__. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential



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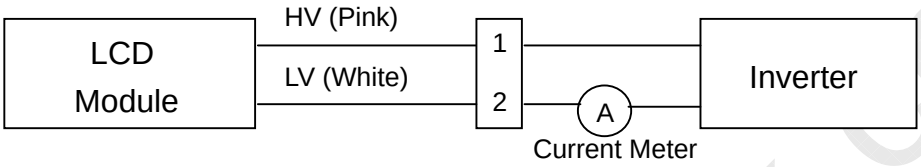
3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	657	730	803	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	7.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	1460 (25 °C)	V_{RMS}	(2)
		-	-	1600 (0 °C)	V_{RMS}	(2)
Operating Frequency	F_L	50	55	60	KHz	(3)
Power Consumption	P_L	3.94	4.38	4.82	W	(4), I_L = 6.0 mA
Lamp Life Time	L_{BL}	15,000	-	-	Hrs	(5)
Leakage Current	I_{IN}-I_{OUT}	-	-	1.3	mA	(7)

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 6.0 mA_{RMS} until one of the following events occurs:

(a) When the brightness becomes ≦ 50% of its original value.

(b) When the effective ignition length becomes ≦ 80% of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within √2 ± 10%;

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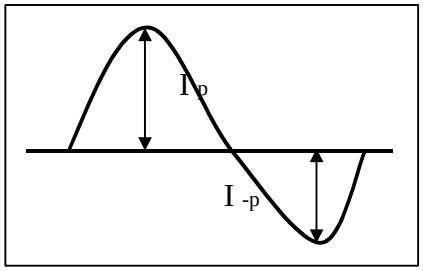
c. The ideal sine wave form shall be symmetric in positive and negative polarities.



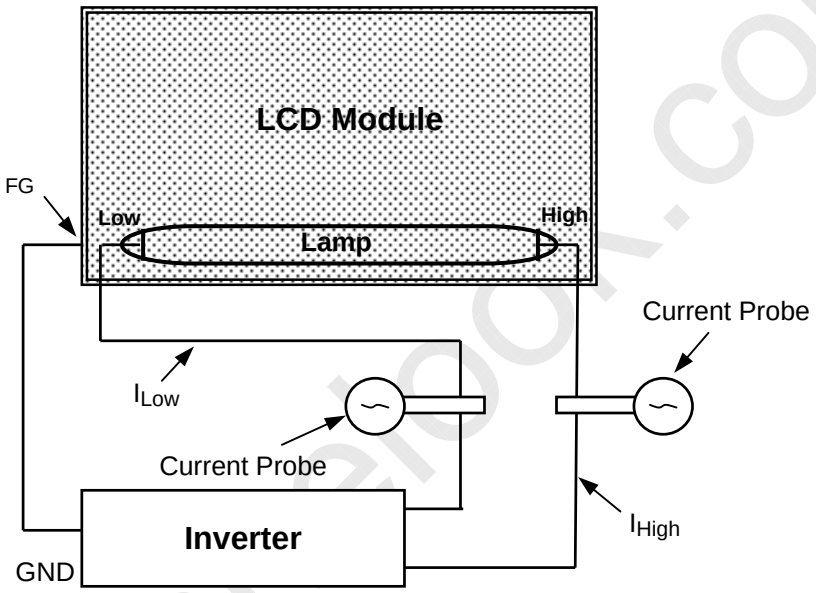
* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

Note (7) The lamp leakage current is measured by the current difference between in and out. And the measurement condition is as below:



$I_{Leak(RMS)} = I_{High(RMS)} - I_{Low(RMS)}$

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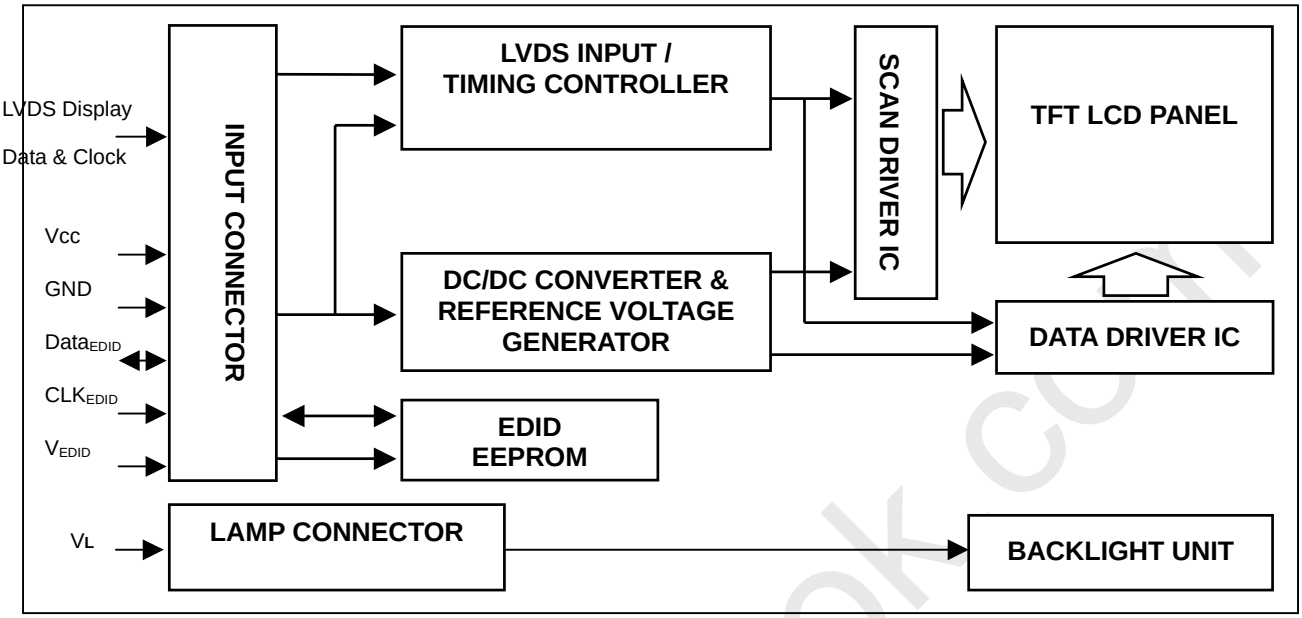
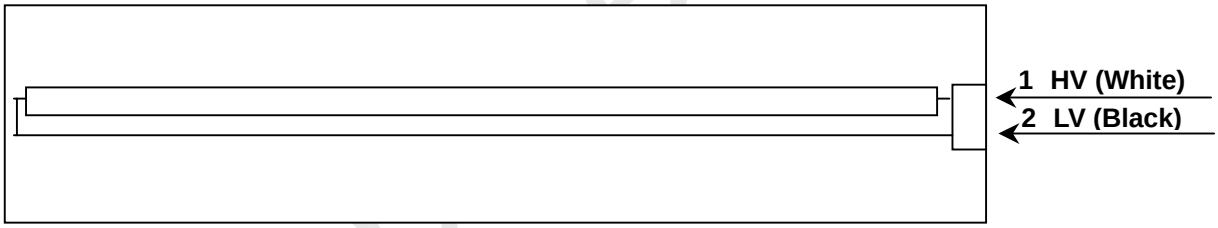
4 BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



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5 INPUT TERMINAL PIN ASSIGNMENT

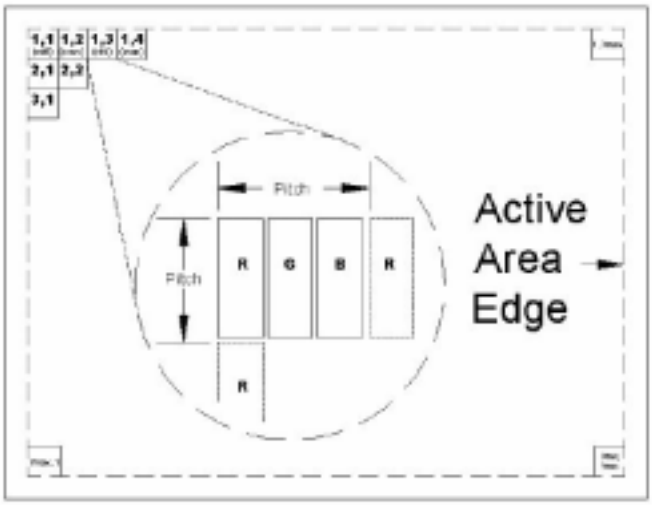
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V_{EDID}	DDC 3.3V Power		
5	NC	Non-Connection		
6	CLK_{EDID}	DDC Clock		
7	$DATA_{EDID}$	DDC Data		
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE-FI-XB30SL-HF11

Note (2) User's connector Part No: JAE-FI-X30C2L

Note (3) The first pixel is odd as shown in the following figure.



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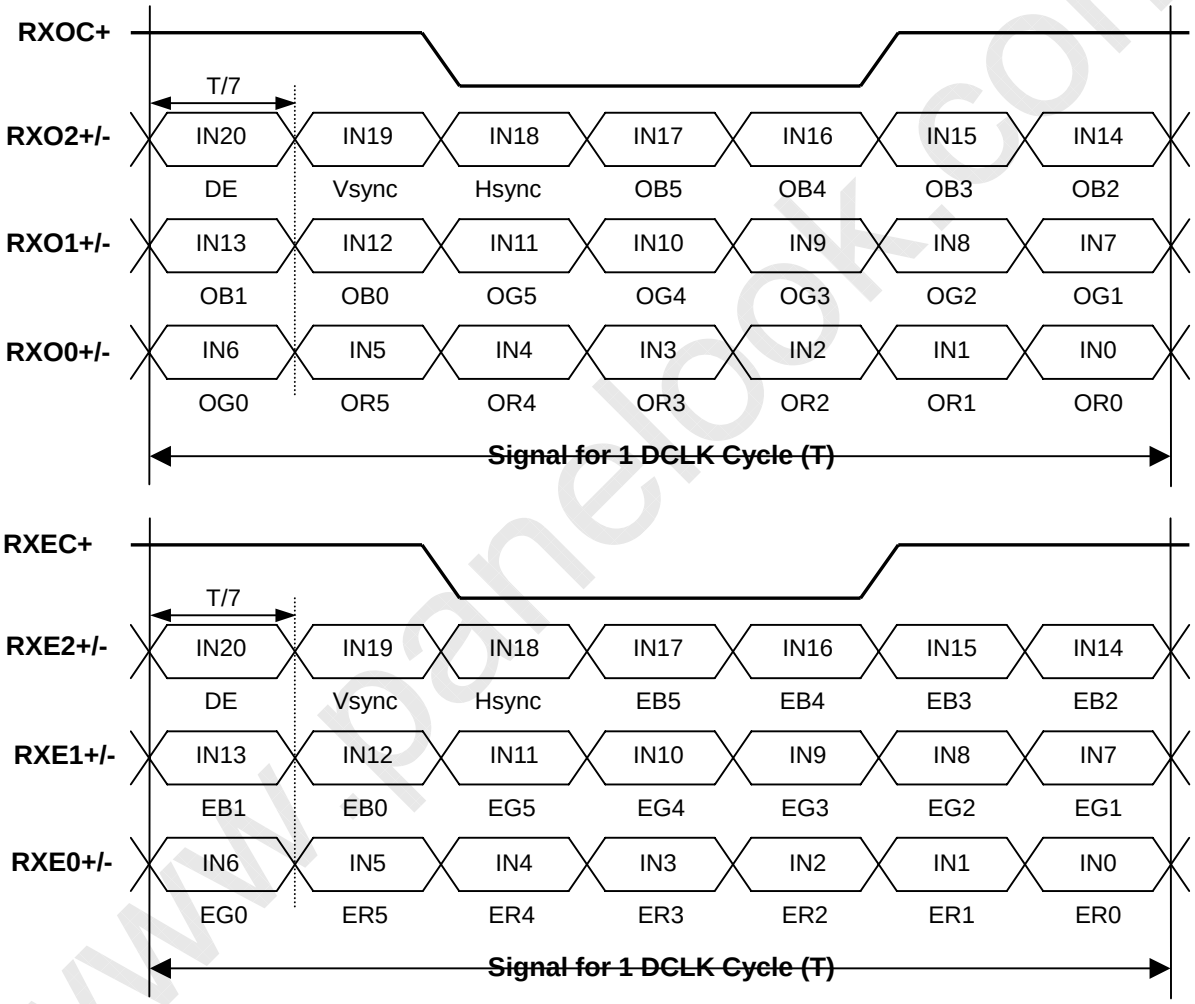
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



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5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N154C1-L01)	45	01000101
11	0B	ID product code (hex LSB first; N154C1-L01)	15	00010101
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	25	00100101
17	11	Year of manufacture (fixed year code)	10	00010000
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Active area horizontal 33.156cm	21	00100001
22	16	Active area vertical 20.7225cm	15	00010101
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	DD	11011101
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	68	01101000
27	1B	Red-x (Rx = “0.593”)	97	10010111
28	1C	Red-y (Ry = “0.337”)	56	01010110
29	1D	Green-x (Gx = ”0.315”)	50	01010000
30	1E	Green-y (Gy = ”0.528”)	87	10000111
31	1F	Blue-x (Bx = ”0.149”)	26	00100110
32	20	Blue-y (By = ”0.119”)	1E	00011110
33	21	White-x (Wx = ”0.307”)	4E	01001110
34	22	White-y (Wy = ”0.316”)	51	01010001
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

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42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“88.75MHz”, According to VESA CVT Rev1.1)	AB	10101011
55	37	# 1 Pixel clock (hex LSB first)	22	00100010
56	38	# 1 H active (“1440”)	A0	10100000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1440 : 160”)	50	01010000
59	3B	# 1 V active (”900”)	84	10000100
60	3C	# 1 V blank (”26”)	1A	00011010
61	3D	# 1 V active : V blank (”900 :26”)	30	00110000
62	3E	# 1 H sync offset (”48”)	30	00110000
63	3F	# 1 H sync pulse width ("32”)	20	00100000
64	40	# 1 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 6”)	00	00000000
66	42	# 1 H image size (”332 mm”)	4C	01001100
67	43	# 1 V image size (”207 mm”)	CF	11001111
68	44	# 1 H image size : V image size (”332 : 207”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name “N154C1-L01”, ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name (“N”)	4E	01001110
78	4E	# 2 2nd character of name (“1”)	31	00110001
79	4F	# 2 3rd character of name (“5”)	35	00110101
80	50	# 2 4th character of name (“4”)	34	00110100
81	51	# 2 5th character of name (“C”)	43	01000011
82	52	# 2 6th character of name (“1”)	31	00110001
83	53	# 2 7th character of name (“-”)	2D	00101101
84	54	# 2 8th character of name (“L”)	4C	01001100
85	55	# 2 9th character of name (“0”)	30	00110000

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86	56	# 2 9th character of name (“1”)	31	00110001
87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with “Blank” character	20	00100000
89	59	# 2 Padding with “Blank” character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor “CMO”, ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string (“C”)	43	01000011
96	60	# 3 2nd character of string (“M”)	4D	01001101
97	61	# 3 3rd character of string (“O”)	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with “Blank” character	20	00100000
100	64	# 3 Padding with “Blank” character	20	00100000
101	65	# 3 Padding with “Blank” character	20	00100000
102	66	# 3 Padding with “Blank” character	20	00100000
103	67	# 3 Padding with “Blank” character	20	00100000
104	68	# 3 Padding with “Blank” character	20	00100000
105	69	# 3 Padding with “Blank” character	20	00100000
106	6A	# 3 Padding with “Blank” character	20	00100000
107	6B	# 3 Padding with “Blank” character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N141C1-L02”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“N”)	4E	01001110
114	72	# 4 2nd character of name (“1”)	31	00110001
115	73	# 4 3rd character of name (“5”)	35	00110101
116	74	# 4 4th character of name (“4”)	34	00110100
117	75	# 4 5th character of name (“C”)	43	01000011
118	76	# 4 6th character of name (“1”)	31	00110001
119	77	# 4 7th character of name (“-”)	2D	00101101
120	78	# 4 8th character of name (“L”)	4C	01001100
121	79	# 4 9th character of name (“0”)	30	00110000
122	7A	# 4 9th character of name (“1”)	31	00110001
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with “Blank” character	20	00100000
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	8C	10001100

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6 INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

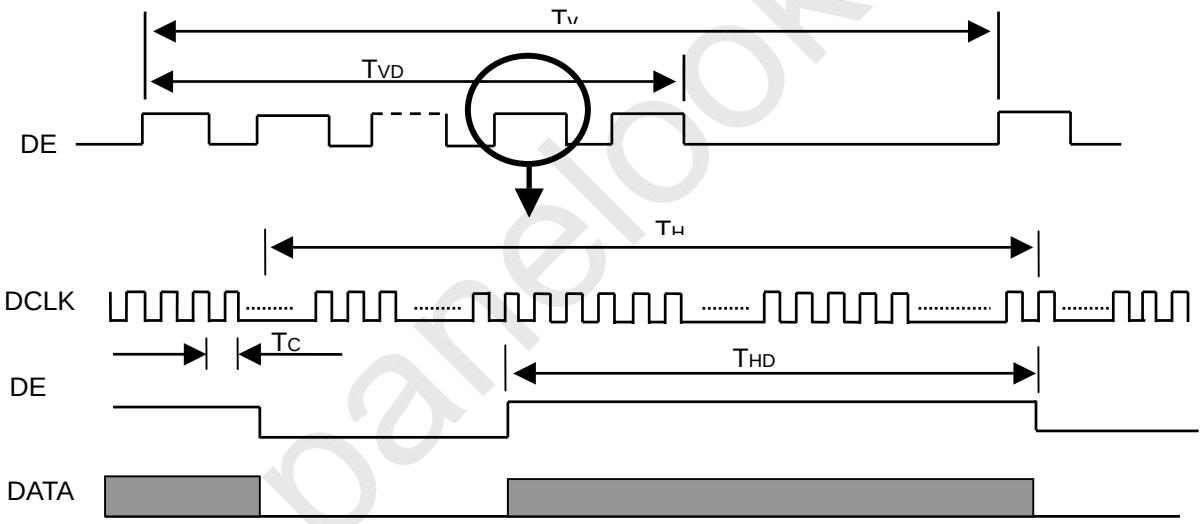
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2)
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	(2)

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM



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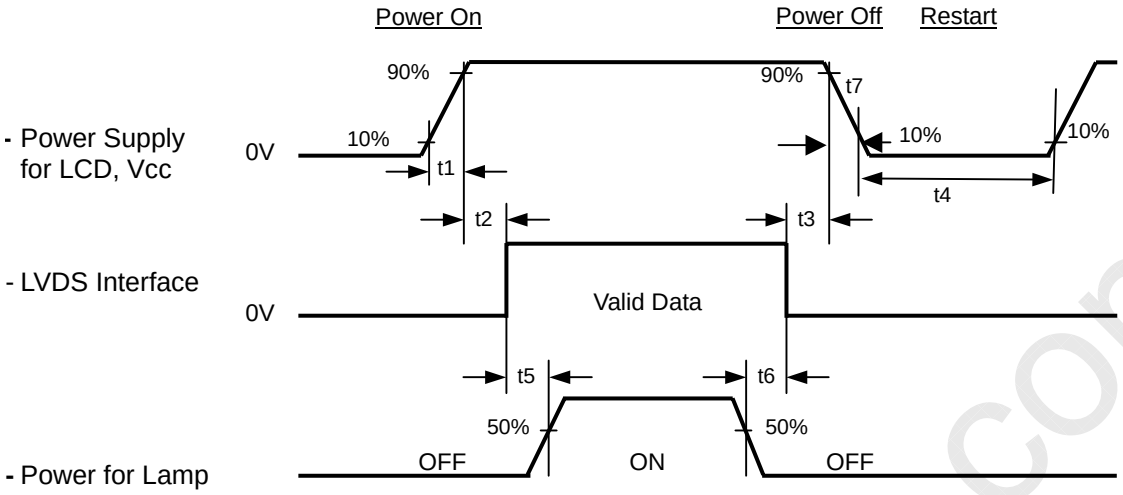
6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 ≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms.

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7 OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I_L	6.0	mA
Inverter Driving Frequency	F_L	**61**	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	**300**	**400**	**-**	-	(2), (5)
Response Time		T_R		**-**	**8**	**12**	ms	(3)
		T_F		**-**	**23**	**28**	ms	
Luminance of White		L_{AVE}		**250**	**300**	**-**	cd/m^2	(4), (5)
White Variation		δW 5pts		-	-	**1.3**	-	(5), (6)
Color Chromaticity	Red	Rx		**TYP -0.03**	**0.592**	**TYP +0.03**	-	(1)
		Ry			**0.338**		-	
	Green	Gx			**0.322**		-	
		Gy			**0.531**		-	
	Blue	Bx			**0.151**		-	
		By			**0.126**		-	
	White	Wx			**0.313**		-	
		Wy			**0.329**		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	**55**	**65**	-	Deg.	
		θ_x-		**55**	**65**	-		
	Vertical	θ_Y+		**40**	**50**	-		
		θ_Y-		**50**	**60**	-		

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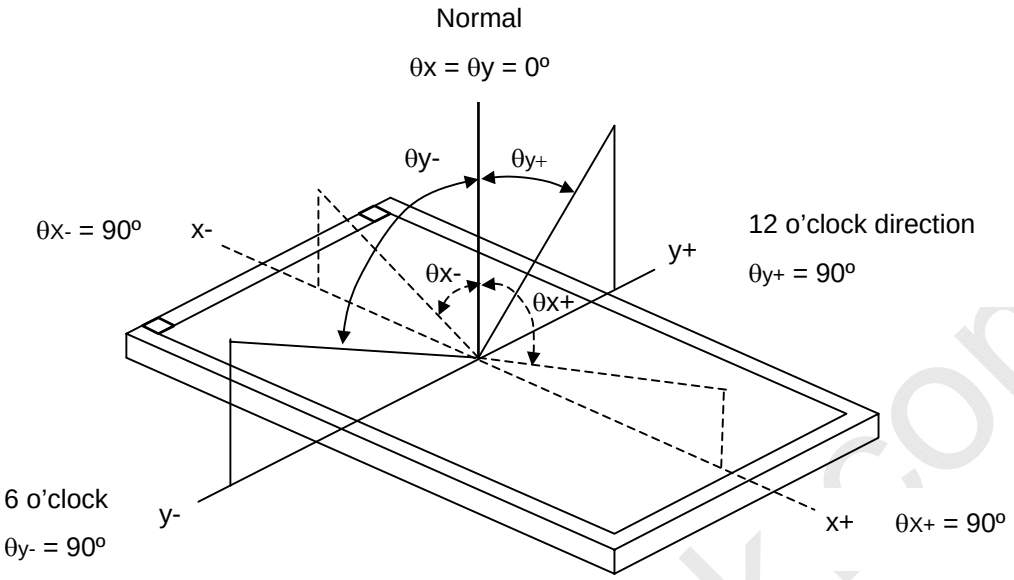
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

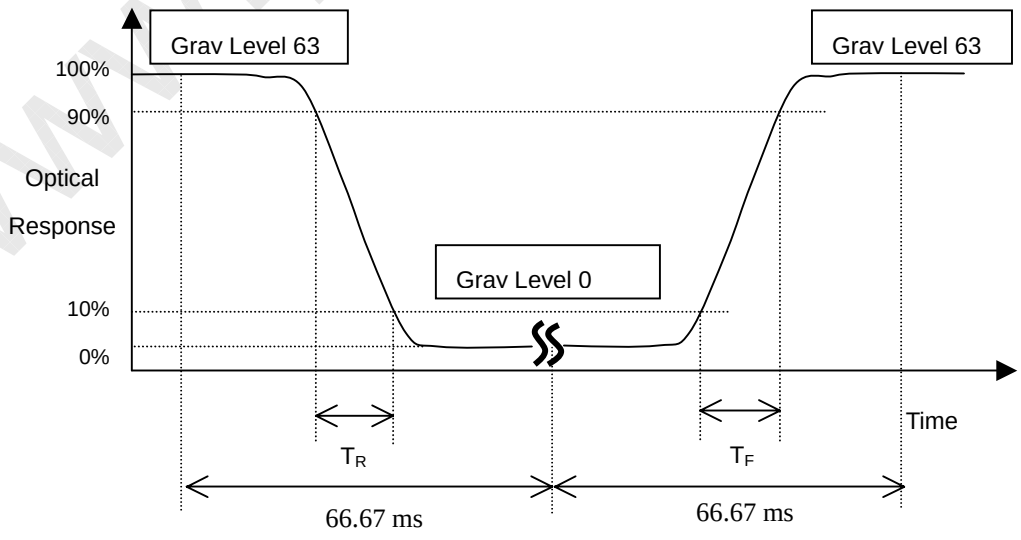
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Average Luminance of White (L_{AVE}):

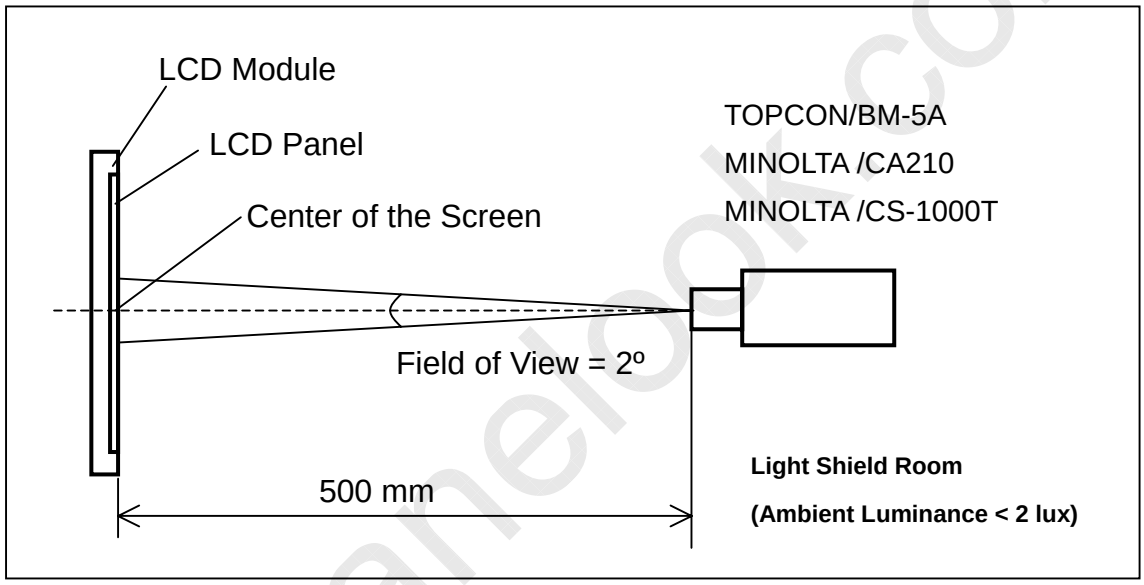
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 15 minutes in a windless room.



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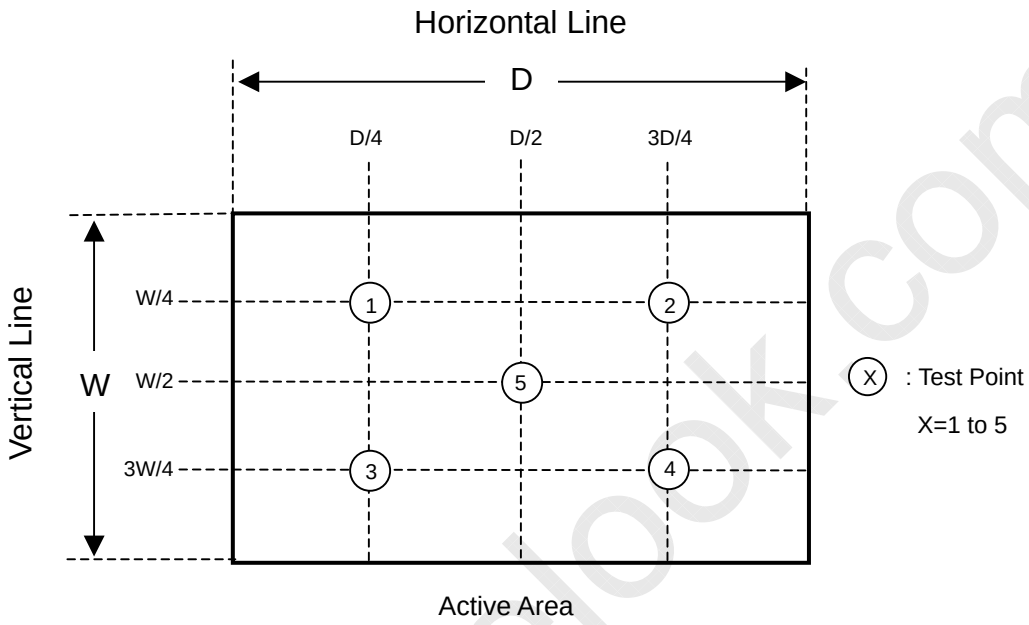
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = Maximum [L (1) ~ L (5)] / Minimum [L (1) ~ L (5)]



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8 PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the lamp wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

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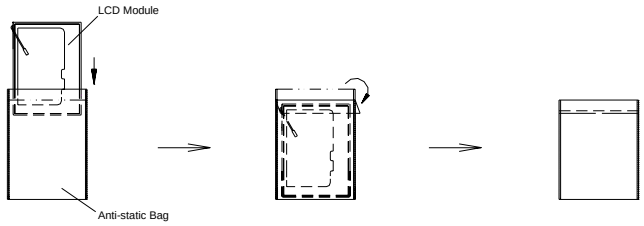
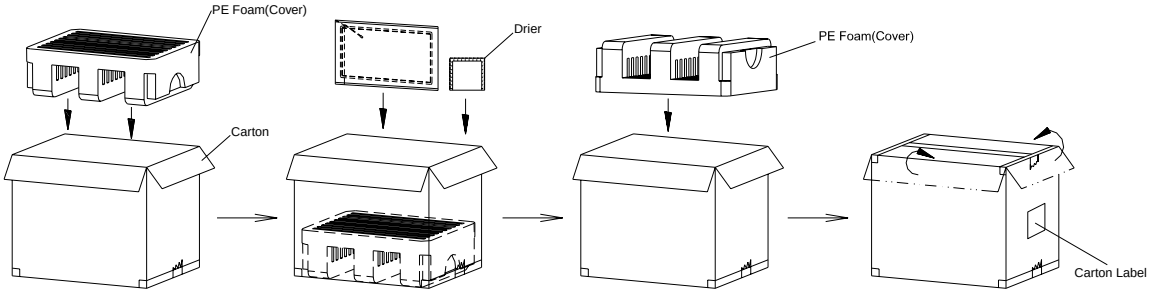
9 PACKING

9.1 CARTON



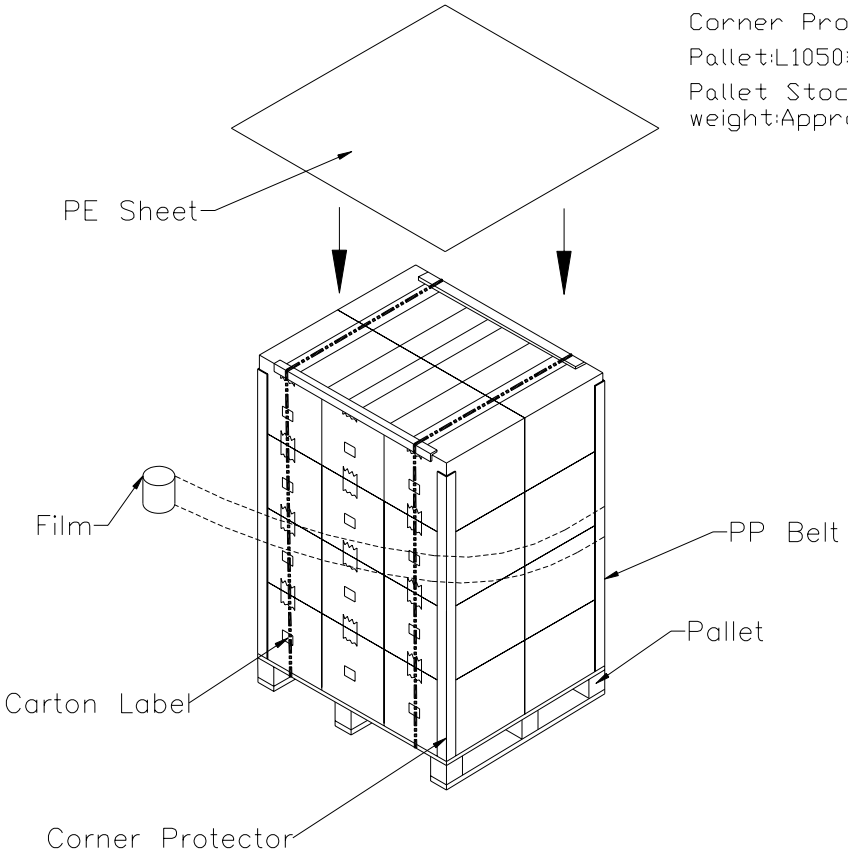
Box dimensions:422(L)x337(W)x355(H)mm

Weight:Appox. 6.9 kg(10 module per 1 box)



9.2 PALLET

Corner Protector:L1350mm*50mm*50mm
Pallet:L1050*W870*H135mm
Pallet Stock Dim:L1050*W870*H1555mm
weight:Approx.185kg



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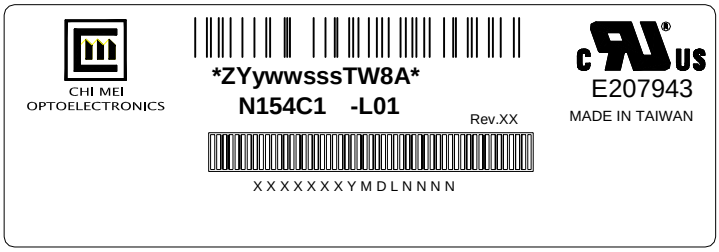
10 DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N154C1 - L01

(b) Revision: Rev. XX, for example: A1, …, C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D X N N N N

- Serial No.
- CMO Internal Use
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

10.2 CARTON LABEL

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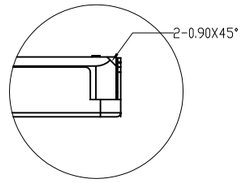
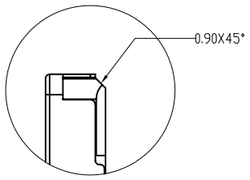
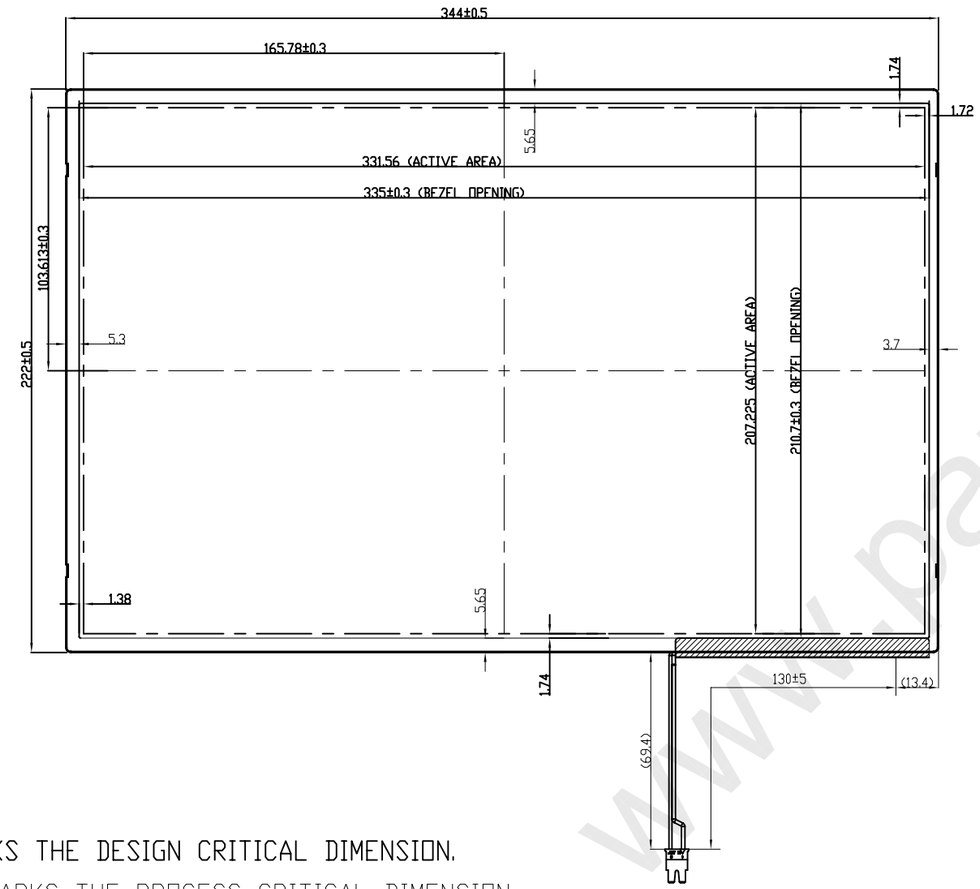
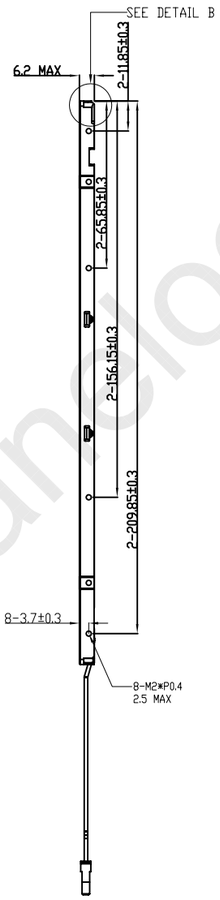


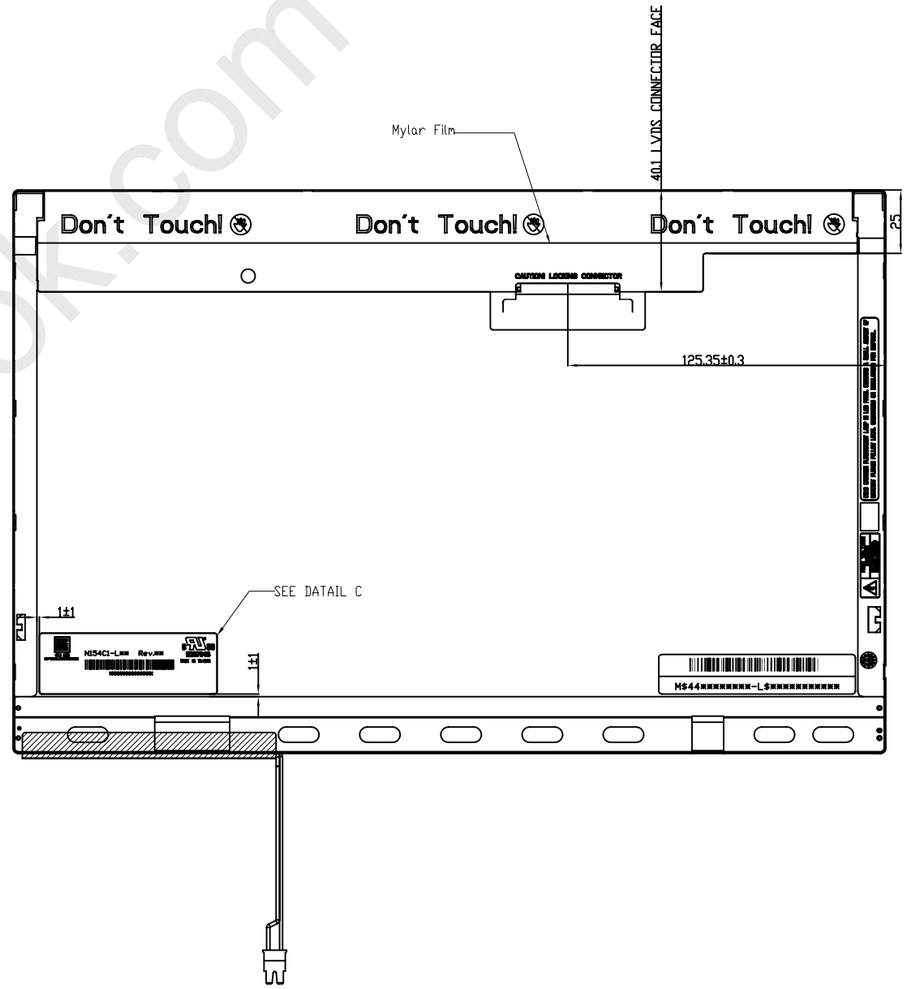
DETAIL A



DETAIL B







NOTES:

1."*" MARKS THE DESIGN CRITICAL DIMENSION.

2." Ⓟ" MARKS THE PROCESS CRITICAL DIMENSION.

3.MAX.SCREW LENGTH: 2.5 mm.

4.MAX.SCREW TORQUE: 2.0 kgf-cm.

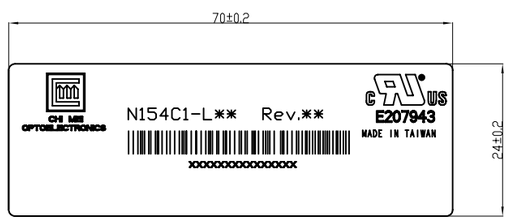
5.SIGNAL INTERFACE CONNECTOR: FI-XB30SRL-HF11 (JAE)

6.CCFL CONNECTOR: BHSR-02VS-1 (JST)

7.Mylar Film :

Base Film : SKC-SH71S t=0.1mm

Adhesive Tape : 3M 467 t=0.05mm



SCALE 2 : 1

DATAIL C

Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark
A	Add new dimension	12-JUL-2006	CHANEY CHEN	CLIFF TSAI		

TITLE	ASSY_MODULE_N154C1 (905)				2D REV.	A
					3D REV.	
Approved	BILL SHEU	Drawing No.	N154B4104A			
Checked	CLIFF TSAI	Part No.	TBD			
Drawer	CHANEY CHEN	Material	TBD	Sheet	1 / 1	A1
Designer	ERIC CHANG	Date	12-JUL-2006	Scale	1:1	Unit:mm

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